CLAIMS

1. A device for protecting a circuit against voltage surges, comprising:

a MOS transistor of a first type connected to first and second supply terminals by its source and its drain, respectively;

a MOS transistor of a second type connected between the second supply terminal and the gate of the transistor of the first type by its source and its drain, respectively; and

a capacitor having a first terminal connected to the first supply terminal and a second terminal connected to the gate of the transistor of the second type.

2. The protection device according to claim 1, wherein a resistor interconnects the gate and the source of each of the transistors of the first and second type.

3. The protection device according to claim 1, further comprising a reverse connected diode between the gate and the source of the transistor of the second type.

4. The protection device according to claim 1, wherein the transistor of the first type is a P-channel transistor, the first supply terminal being a positive supply terminal.

5. The protection device according to claim 2, wherein the transistor of the first type is a P-channel transistor, and the first supply terminal is a positive supply terminal.

6. The protection device according to claim 3, wherein the transistor of the first type is a P-channel transistor, and the first supply terminal is a positive supply terminal.

7. A circuit comprising:

a first transistor having a first terminal coupled to a first supply voltage and a second terminal coupled to a second supply voltage;

a second transistor having a first terminal coupled to a third terminal of said first transistor and a second terminal coupled to said second supply voltage; and

a capacitor coupled between a third terminal of said second transistor and said first

supply voltage.

8. The circuit of claim 7, further comprising a diode coupled between said third terminal of said second transistor and said second supply voltage.

9. The circuit of claim 7, further comprising a first resistor coupled between said third terminal of said first transistor and said first voltage supply.

10. The circuit of claim 9, further comprising a second resistor coupled between said third terminal of said second transistor and said second voltage supply.

11. The circuit of claim 8, wherein an anode of said diode is coupled to said third terminal of said second transistor, and a cathode of said diode is coupled to said second voltage supply.

12. The circuit of claim 7, wherein said first transistor and said second transistor are of the MOS type.

13. The circuit of claim 11, wherein said first transistor comprises a P-channel, MOS transistor, and said first, second and third terminals of said first transistor are its source, drain and gate, respectively, said second transistor comprises an N-channel, MOS transistor, and said first, second and third terminals of said second transistor are its drain, source and gate, respectively, and wherein said first voltage supply is positive and said second supply voltage is negative.

14. The circuit of claim 11, wherein said first transistor comprises an N-channel, MOS transistor, and said first, second and third terminals of said first transistor are its drain, source and gate, respectively, said second transistor comprises a P-channel, MOS transistor, and said first, second and third terminals of said second transistor are its source, drain and gate, respectively, and wherein said first voltage supply is negative and said second supply voltage is positive.

15. A device for protecting a circuit against voltage surges comprising:

a first transistor having a first terminal coupled to a first power supply and a second terminal coupled to a second power supply;

a second transistor having a first terminal coupled to said first power supply and a second terminal coupled to said second power supply and to a third terminal of said first transistor; and

a third transistor having a first terminal and a third terminal coupled to said first power supply and a second terminal coupled to said second power supply and to a third terminal of said second transistor;

wherein said third terminals of said first, second and third transistors are coupled to said second power supply through first, second and third resistors, respectively.

16. The device of claim 15, wherein said third terminal of said third transistor is coupled to said first power supply through a capacitor.

17. The device of claim 16 wherein said first, second and third transistors are NPN bipolar transistors.

18. A device for protecting a circuit from voltage surges comprising:

first and second means for switching coupled between a first power supply and a second power supply;

a capacitor coupled between said first means for switching and said first power supply;

a first resistor coupled between said first means for switching and said second power supply; and

a second resistor coupled between said second means for switching and said first power supply;

wherein, upon the occurrence of a voltage surge on said first power supply, said first means for switching closes, thereby supplying a voltage to said second means for switching, which also closes, thereby causing a short-circuit between said first and second voltages.

19. The device of claim 18, further comprising a third means for switching coupled between said first means for switching and said second power supply.

20. The device of claim 19, wherein said first means for switching comprises a transistor of a first type, said second means for switching comprises a transistor of a second type and said third means for switching comprises a diode.

21. The device of claim 20, wherein said transistor of a first type comprises an N-channel MOS transistor.

22. The device of claim 21, wherein said transistor of a second type comprises a P-channel MOS transistor.

23. A device for protecting a circuit against voltage surges comprising:

a first means for switching having a first terminal coupled to a first power supply and a second terminal coupled to a second power supply;

a second means for switching having a first terminal coupled to said first power supply and a second terminal coupled to said second power supply and to a third terminal of said first means for switching; and

a third means for switching having a first terminal and a third terminal coupled to said first power supply and a second terminal coupled to said second power supply and to a third terminal of said second means for switching;

wherein said third terminals of said first, second and third means for switching are coupled to said second power supply through first, second and third resistors, respectively.

24. The device of claim 23, wherein said third terminal of said third means for switching is coupled to said first power supply through a capacitor.

25. The device of claim 24, wherein said first, second and third means for switching are NPN bipolar transistors.

26. A method for protecting a circuit from voltage surges, the method

comprising the steps of:

supplying a voltage from a first power supply to a first switch means;

wherein, upon the occurrence of a voltage surge on said first power supply, said first switch means ~~supplying~~ power from a second power supply to a second switch means; and said second switch means short-~~circuiting~~ said first and second power supplies in order to alleviate said voltage surge.